Subject	Computer Organ./Architect	**Course Code**	CT115	**Theoretical**	4 hrs / wk
Semester	2	**Prerequisite**	IT100	**Practical**	0 hrs / wk

Objective: To Provide the opportunity to Understand Structure of Computers to be able to utilize architecture to develop System Program		
Week 1	**Topic**	**Description**
	1. Introduction and Terms. 2. Computer Hardware Units. 3. Computer Software. 4. The Software Development Cycle.	Including The Subject of Computer architecture and organization. General view and Von-Nueman architecture highlighting program tasks and components, software development environment and producing executable machine code.
Week 2	**Topic**	**Description**
	1. Computer Description. 2. Computer main functions and data flow. 3. Performance criteria CISC Computer and Risk Computers. 4. Technology Constraint.	Explaining the architecture versus Organization Structure versus function. The main function of computers. Computer classification into Microcomputer versus Minicomputers and technology constraint for each class.
Week 3	**Topic**	**Description**
	1. Central processing unit. 2. The functions the CPU. 3. The role of the control unit in the CPU 4. Internal CPU buss and the external system bus.	The structure of the CPU : ALU , CU , General Register , Special Register and Buses . Introduction the function of the CPU , Then knowing how the CPU synchronizes its functions internally and externally by the control unit and the system bus.
Week	**Topic**	**Description**

4	1. Case Study: the architecture organization for Intel 8086 microprocessor. 2. Intel 8086 CPU. 3. Intel 8086 Flag Register.	Introduction and analyzing the Intel 8086 CPU architecture: Bus interface Unit BIU, Execution Unit EU and operations Parallelism. Example in assembly how flags are affected by instructions.
Week 5	**Topic**	**Description**
	1. Memory organization and the physical address calculation. 2. Interrupt system in Intel 8086.	How the main memory for 8086 cpu is organized and divided into segments. and how is the address space in mapped into a virtual space with physical address calculation mechanism. Then the student should know the interrupts , vectors and handling.
Week 6	**Topic**	**Description**
	1. Instructions Execution and Sequencing. 2. Machine code programming. 3. Instruction fetching and executing cycle. 4. Instruction format.	Explaining how the CPU executes and instructions from decoding the instruction format and interrupting the meaning of the instruction. This is well demonstrated using a sample from machine code programming: Op-code field and operand(s) field.
Week 7	**Topic**	**Description**
	1. Instruction sequencing state diagram. 2. Operations done by the instruction. 3. CPU tasks to complete the execution of an instruction. 4. Place of data to be manipulated.	Following how a CPU completes the execution of an instruction. What stages to follow and what the operations are done by the instruction. Where data can be found to be manipulated as sources of information.
Week 8	**Topic**	**Description**
	1. Immediate addressing mode. 2. Direct and indirect addressing mode. 3. Register and register indirect addressing mode.	Introduction and analyzing various addressing modes used by most architectures. Examples are taken from addressing modes used by Intel 8086 CPU for real

	4. Displacement and stack addressing mode.	demonstration. Other addressing modes can be easily derived from those mentioned addressing mode.
Week 9	**Topic**	**Description**
	1. Mid Term Exam.	Testing the knowledge gained by students so far.
Week 10	**Topic**	**Description**
	1. Memory hierarchy and performance factors. 2. Semi conductors memory. 3. Memory cell Structure.	Memory organization. Memory as a store for programming and data: RAM, ROM, PROM, EPROM, EEPROM, Flash memory, Data line, Control line and select line and the bit storage media.
Week 11	**Topic**	**Description**
	1. Mapping techniques: Direct mapping, set associative mapping and full associative mapping. 2. Replacement strategies: FIFO, LRU, LFU. 3. Write policies: write back write through.	Cash memory organization and management. Example for mapping techniques, replacement strategies and write policies.
Week 12	**Topic**	**Description**
	1. Mechanisms for data input and output. 2. Memory mapped devices and isolated addressed device. 3. Programming and interrupted input/output.	Input and output techniques handling. Introducing the concept of device interface. Highlighting how devices are treated from the software point of view: example for each method.
Week 13	**Topic**	**Description**
	1. Direct memory access (DMA). 2. DMA controller architecture. 3. DMA programming and functions.	Introducing the concept, general structure and comparing and outputting using DMA.
Week	**Topic**	**Description**

14	1. External buses classifications. 2. PC2 bus structure and operations. 3. ISA and EISA bus structures, attributes and functionality. 4. USB features, structures.	System bus architectures. Introducing and comparing different buses structures.

Course Assessment:

Mid Term	Lap Activities	Final Exam
25%	15%	60%

Text Box and References:

1. "Computer Architecture and Organization" john P.Hayes, 2nd Edition.
2. "The Intel Microprocessor 8086/80286…/Pentium Pro Processor: Architecture Programming and Interfacing" Barry B.Bary, 5th Edition 2000.